

1 What is claimed is:

- 1. A method of forming a portion of a semiconductor integrated circuit;
- 3 comprising the steps of:
- growing a field oxide across the integrated circuit;
- patterning and etching the field oxide to form an opening with substantially 6 vertical sidewalls exposing a portion of an upper surface of a substrate underlying the 7 field oxide where an active area will be formed;
- growing a gate oxide over the exposed portion of the substrate;
- depositing a polysilic on layer over the field oxide and gate oxide to a thickness
 wherein the lowest most portion of the upper surface of the polysilicon is above the
 upper surface of the field oxide;
- planarizing the polysilicon layer;
- forming a photoresist mask over a portion of the polysilicon layer overlying at 14 least a portion of the substrate not covered by the field oxide;
- patterning and etching the polysilicon and gate oxide to form a gate electrode;

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- forming sidewall spacers along the sides of the gate electrode.
- 2. The method of claim 1, wherein the field oxide has a thickness of between 4 approximately 4000-5000 angstroms.
- 3. The method of claim 1, further comprising the steps of:
- forming an name in the substrate before the field oxide is formed in areas where the field oxide will be removed.
- 4. The method of claim 3, wherein the n-well is formed by implantation and 9 drive-in of phosphorous.
- 5. The method of claim 1, further comprising the step of:
- performing a blanket implant in the substrate to adjust to desired doping levels labeling before forming the gate oxide layer.
- 13 6. The method of claim 5, wherein the blanket implant comprises boron 14 implanted at a dosage of approximately 1.5 X 10¹²/cm² at 30 KeV.

- 7. The method of claim 6, further comprising the steps of:
- 2 masking off the p-type regions, and
- performing a punch-through implant into the n-well regions.
- 8. The method of claim 7 wherein the punch-through implant comprises boron 5 implanted at a dosage of approximately 1 X 10¹²/cm² at approximately 75 KeV.
- 9. The method of claim 5, further comprising the steps of:
- 7 masking off selected p-type regions in the substrate; and
- implanting dopants into selected n-wells to further adjust the doping levels of the n-wells and not the selected p-type regions in the substrate.
- 10. The method of claim 9, wherein the dopant comprises boron implanted at a 11 dosage of approximately 1.7 X 10¹²/ cm² and at approximately 30 KeV.

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- 11. The method of claim 1, further comprising the steps of:
- 2 masking off selected n-well regions in the substrate; and
- implanting a dopant into the p-type regions to adjust to a desired doping level.
- 12. The method of claim 11, wherein the dopant comprises boron implanted at a 5 dosage of approximately 6 X 10 2 on 2 and at approximately 180 KeV.
- 13. The method of claim 1, wherein the gate oxide has thickness of between 7 approximately 70-100 angstroms.
- 8 14. The method of claim 1, wherein the polysilicon layer is formed to a thickness 9 of between approximately 7000-9000 angstroms.
- 15. The method/of claim 1, wherein the polysilicon is in-situ doped as deposited.
- 11 16. The method of claim 1, further comprising the step of:
- doping the polysilicon to a desired doping level after deposition.

- 1 17. The method of claim 1, wherein the step of planarizing the polysilicon 2 comprises CMP.
- 18. The method of claim 1, wherein the step of planarizing the polysilicon 4 comprises the steps of:
- forming a planar layer over the polysilicon layer having an etch ratio of 1:1 with 6 the polysilicon;
- 7 performing an etchback of the planar layer and polysilicon.
- 8 19. The method of claim 18, wherein the planar layer is spin-on-glass.
- 9 20. The method of claim 18, wherein the planar layer is photoresist.
- 21. The method of claim 18, wherein the etchback comprises a wet etch.
- 11 22. The method of claim 18, wherein the etchback comprises chemical 12 mechanical polishing.
- 23. The method of claim 18, wherein there remains a layer of polysilicon above 14 the surface of the field oxide and in the opening after the polysilicon is etched.

- 1 24. The method claim 23, wherein the remaining polysilicon is approximately 2 1500-2000 angstroms over the field oxide.
- 25. The method of claim 18, wherein the upper surface of the polysilicon is 4 substantially planar with an upper surface of the field oxide.
- 5 26. The method of claim 1, further comprising the step of:
- forming an etch stop layer over the field oxide before the polysilicon layer is 7 formed.
- 8 27. The method of claim 24, wherein the etch stop layer comprises nitride.
- 9 28. The method of claim 1, further comprising the step of:
- forming a silicide layer over the polysilicon, the substrate and the field oxide 11 before the photoresist is formed; and
- etching the silicide with polysilicon.

30. The method of claim 28, wherein the silicide has a thickness of between 4 approximately 1200-1700 angstroms.

- 5 31. The method of claim 1, further comprising the step of:
- forming a capping layer over the polysilicon layer before the photoresist is 7 formed; and
- 8 etching the silicide along with the polysilicon.
- 9 32. The method of claim 31, wherein the capping layer comprises oxide.
- 33. The method of claim 31, wherein the capping oxide has a thickness of 11 between approximately 1200-1700 angstroms.
- 34. The method of claim 1, further comprising the step of:
- forming lightly doped drain regions in the substrate adjacent the gate electrode 14 before the sidewall spacers are formed.

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- forming source/drain regions in the substrate adjacent the gate electrode after
- 3 the sidewall spacers are formed.
- 4 36. The method of claim 1, further comprising the steps of:
- forming a raised source/drain region adjacent the gate electrode and overlying 6 the exposed substrate.

- 37. The method of claim 36, wherein the step of forming a raised source/drain further comprises the steps of:
- forming a capping layer over the polysilicon layer before the photoresist is 4 formed;
- etching the capping layer with the polysilicon layer;
- depositing a polysticon layer over the transistor gate electrode, exposed

 7 substrate and the field oxide wherein the lowest most portion of the upper surface of the

 8 polysilicon layer is above the upper surface of the gate electrode;
- 9 forming a planar sacrificial layer over the polysilicon layer having a 1:1 etch rate 10 with the polysilicon layer;
- etching the sacrificial layer and the polysilicon layers exposing the upper surface 12 of the field oxide;
- doping the polysilicon layer to a desired doping level.
- 38. The method of claim 37, wherein the lowest most portion of the upper surface of the polysilicon layer is above the upper surface of the gate electrode.

- 39. The method of claim 37, further comprising the step of:
- forming a silicide under the capping layer and over the polysilicon before the polysilicon is deposited.
- 4 40. The method of claim 36, wherein the step of forming a raised source/drain 5 further comprises the steps of:
- selectively growing epitaxy above the exposed substrate surface;
- 7 implanting the epitaxy with an appropriate dopant to achieve a desired 8 conductivity level; and
- 9 siliciding an upper portion of the selectively grown epitaxy.

- 41. A method of forming/a portion of a semiconductor integrated circuit; 1
- 2 comprising the steps of:
- growing a field oxide/across the integrated circuit; 3
- patterning and etohing the field oxide to form an opening with substantially 4
- 5 vertical sidewalls exposing a portion of an upper surface of a substrate underlying the
- 6 field oxide where an active area will be formed;
- growing a gafe oxide over the exposed portion of the substrate; 7
- depositing a doped polysilicon layer over the field oxide and gate oxide to a 8
- 9 thickness wherein the lowest most portion of the upper surface of the polysilicon is
- 10 above the upper/surface of the field oxide;
- planarizing and etching the polysilicon layer such that the upper surface of the 11
- 12 polysilicon layer remains at or above the upper surface of the field oxide;
- forming a silicide over the polysilicon layer; 13
- forming a capping layer over the silicide; 14

- forming a photoresist mask over a portion of the capping layer overlying at least 2 a portion of the substrate not covered by the field oxide;
- patterning and etching the capping layer, the silicide, the polysilicon and gate 4 oxide to form a gate electrode of a transistor;
- 5 removing the photoresist;
- forming LDD regions in the substrate adjacent the gate electrode;
- forming sidewall spacers along the sides of the gate electrode; and
- forming source/drain regions adjacent the gate electrode.
- 9 42. The method of claim 41, further comprising the step of:
- forming n-wells in the substrate before the field oxide is formed in areas where 11 the field oxide will be removed.
- 12 43. The method of claim 41, wherein the polysilicon layer is formed to a 13 thickness of between approximately 7000-9000 angstroms.

- 1 44. The method of claim 41, wherein the silicide is formed from the group 2 consisting of tantalum, tungsten, titanium and molybdenum.
- 45. The method of claim 41, wherein the silicide has a thickness of between 4 approximately 1200-1700 angstroms.
- 5 46. The method of claim 41, wherein the capping layer has a thickness of 6 between approximately 1200-1700 angstroms.
- 7 47. The method of claim 41, further comprising the step of:
- forming a raised source/drain region adjacent the gate electrode and overlying 9 the exposed substrate.

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- 1 50. The structure of claim 48, further comprising:
- an n-well in the active area in the substrate.
- 51. The structure of claim 48, wherein the gate oxide has a thickness of 4 between approximately 70-100 angstroms.
- 5 52. The structure of claim 48, wherein the polysilicon gate electrode has a 6 thickness of between approximately 7000-9000 angstroms.
- 7 53. The structure of claim 48, further comprising:
- a silicide layer over the polysilicon gate electrode.
- 9 54. The structure of claim 53, wherein the silicide is from the group consisting of 10 tantalum, tungsten, titanium and molybdenum.
- 11 55 The method of claim 53, wherein the silicide has a thickness of between 12 approximately 1200-1700 angstroms.

- 48. A structure consisting of a portion of a semiconductor integrated circuit,
- 2 comprising:
- a field oxide formed across the integrated circuit having an opening therethrough
- 4 with substantially vertical sidewalls exposing a portion of an upper surface of a
- 5 substrate underlying the field oxide;
- a gate oxide over portion of the exposed portion of the substrate;
- a polysilicon gate electrode overlying the gate oxide and having an upper
- g surface planar with or above an upper surface of the field oxide;
- 9 LDD regions in the substrate adjacent the gate electrode; and
- sidewall spacers along the sides of the polysilicon gate electrode.
- 11 49. The structure of claim 48, wherein the field oxide has a thickness of between
- 12 approximately 4000-5000 angstroms.
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a capping layer over the silicide.

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57. The structure of claim 56, wherein the capping layer comprises oxide.

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58. The structure of claim 56, wherein the capping layer has a thickness of

5 between approximately 1200-1700 angstroms.

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59. The structure of claim 48, further comprising:

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LDD regions in the substrate adjacent the gate electrode.

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60. The structure of claim 48, further comprising:

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source/drain regions adjacent the gate electrode in the substrate.

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61. The structure of claim 48, further comprising:

- raised source/drain regions adjacent the gate electrode and overlying the
- 12 exposed substrate.

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- 62. The structure of claim 61, wherein the raised source/drain regions comprise:
- 2
- doped polysilicon; and
- 3
- silicide over the upper surface of the doped polysilicon.
- 4
- 63. The structure of claim 61, wherein the raised source/drain regions comprise:
- 5
- doped sele¢tively grown epitaxy; and
- 6
- silicide over an upper portion of the selectively grown epitaxy.
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- 1 64. A structure consisting of a portion of a semiconductor integrated circuit, 2 comprising:
- a field oxide formed across the integrated circuit having an opening therethrough 4 with substantially vertical sidewalls exposing an active area in a portion of an upper 5 surface of a substrate underlying the field oxide;
- a gate oxide over a portion of the exposed substrate;
- a polysilicon gate electrode overlying the gate oxide and having an upper surface planar with or above the upper surface of the field oxide;
- 9 a silicide layer over the polysilicon layer;
- a capping layer over the silicide layer;
- LDD regions in the substrate adjacent the gate electrode; and
- sidewall spacers along the sides of the polysilicon gate electrode.

- 1 65. The structure of claim 64, further comprising:
- 2 source/drain regions adjacent the gate electrode.
- 3 66. The structure of claim 65, wherein the source/drain regions are in the 4 substrate.
- 5 67. The structure of claim 64, wherein the source/drain regions comprise:
- a raised doped polysilicon layer over the exposed substrate and adjacent to the gate electrode.
- 8 68. The structure of claim 64, wherein the source/drain regions comprise:
- a raised doped selectively grown epitaxial region over the exposed substrate surface and adjacent to the gate electrode; and
- a silicide over an upper portion of the epitaxial region.

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